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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No.	042390.P6139C
First Inventor or Application Identifier	Ellissa E. Carapella
Title	SPLIT CAVITY WALL PLATING FOR AN INTEGRATED CIRCUIT
Express Mail Label No.	EL466331065US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification [Total Pages 15]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) *(35 U.S.C. 113)* [Total Sheets 3]

4. Oath or Declaration [Total Pages 3]
a. ☐ Newly executed (original copy)
b. ☒ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
9. ☐ English Translation Document *(if applicable)*
10. ☐ Information Disclosure Statement (IDS)/PTO - 1449 ☐ Copies of IDS Citations
11. ☒ Preliminary Amendment
12. ☐ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ *Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☐ Other: .....

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: 09/153,630

Prior application Information: Examiner Mancho, R. Group/Art Unit: 3661

For CONTINUATION or DIVISIONAL APPS only The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Label (Insert Customer No. or Attach bar code label here) or ☒ Correspondence address below

Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
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Country	U.S.A.	Telephone	(714) 557-3800	Fax	(714) 557-3347

Name (Print/Type)	William E. Alford, Reg. No. 37,764		
Signature		Date	09/19/00

Burden Hour Statement This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

Our Docket No.:042390.P6139C
Express Mail No.: EL466331065US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: CARAPELLA, et al. Serial No.: Unassigned Filed: 09/19/00 For: SPLIT CAVITY WALL PLATING FOR AN INTEGRATED CIRCUIT PACKAGE	Examiner: Unassigned Art Group: Unassigned
Which is a Continuation of: CARAPELLA, et al. Serial No.: 09/153,630 Filed: 09/15/98 For: SPLIT CAVITY WALL PLATING FOR AN INTEGRATED CIRCUIT PACKAGE	

PRELIMINARY AMENDMENT
ACCOMPANYING
35 USC 120 and 37 CFR 1.53(b)(1) CONTINUATION APPLICATION

Assistant Commissioner for Patents
Washington, DC 20231-9998

Dear Sir:

Prior to a first examination in the 35 USC 120 and 37 CFR 1.53(b)(1) continuation application filed herewith, please enter the following amendments:

IN THE SPECIFICATION

Page 1, line 1, before "BACKGROUND OF THE INVENTION" please insert the following paragraph:

--CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of and is a continuation of Application No. 09/153,630, filed September 15, 1998, now issued as U.S. Patent No. _____.--

REMARKS

Prior to a first examination, please enter the foregoing amendments.

The application papers filed herewith are a true copy of the prior complete application filed on September 15, 1998 having Application No. 09/153,630. Pursuant to 35 U.S.C. 120 and 37 CFR 1.78(a), this continuation application filed under 37 CFR 1.53(b) claims the benefit of and is a continuation of Application No. 09/153,630, filed September 15, 1998.

Claim 1-16 remain at issue in the application. Applicant believes that no new matter has been added through these amendments.

CONCLUSION

Examination is respectfully requested. Allowance of the claims at an early date is hereby respectfully solicited.

The examiner is invited to contact Applicant's undersigned counsel by telephone at (714) 557-3800 to expedite the prosecution of this case should there be any unresolved matters remaining.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: September 19, 2000

William E. Alford
Reg. No. 37,764

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: September 19, 2000.

Susan McFarlane 9/19/00
Susan McFarlane *Date*

12400 Wilshire Boulevard,
Seventh Floor
Los Angeles, California 90025
(714) 557-3800

Our File No.: 042390.P6139
Express Mail No.: EL105935232US

UNITED STATES PATENT APPLICATION

FOR

SPLIT CAVITY WALL PLATING FOR AN INTEGRATED CIRCUIT PACKAGE

INVENTORS: Elissa E. Carapella
Mark J. Palmer

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 Wilshire Blvd., 7th Floor
Los Angeles, CA 90025-1026
(714) 557-3800

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to an integrated circuit package.

2. DESCRIPTION OF RELATED ART

Integrated circuits are typically housed within a package which has a plurality of external contacts that are soldered to a printed circuit board. The package may also have a number of internal bond pads that are connected to corresponding pads of the integrated circuit by bond wires or a tape automated bonding (TAB) tape. The internal bond pads may be connected to the external contacts by routing layers and busses within the package. The busses and routing layers have conductive planes and traces that are dedicated to the power/ground busses and digital signal lines of the integrated circuit, respectively. By way of example, a conventional package may have a first bus layer dedicated to power, one or more routing layers dedicated to digital signals and a second bus layer dedicated to ground.

The various conductive layers are spatially located within different planes in the package. The layers are typically interconnected by conductive vias formed within the package. The bond pads may also be connected to the internal

conductive layers by vias. Vias are typically formed by creating a hole in the dielectric package material and then plating the hole with a conductive material such as copper. The plating process is a relatively time consuming and expensive step. For this reason it is desirable to create an integrated circuit package with a minimal number of vias.

Some integrated circuits require power at different voltage levels. For example, an integrated circuit may require both 3.3 V and 2.0 V power. The additional voltage level requires an additional conductive power plane within the package. The second power plane can be created by forming an additional conductive layer within the package. The additional conductive layer requires more vias to connect the second power plane to the bond pads. It would be desirable to provide a dual voltage integrated circuit package which minimized the number of vias required to interconnect the pads and conductive layers of the package.

U.S. Patent No. 5,557,502, issued to Banerjee et al., discloses an integrated circuit package which has a conductive strip that wraps around an edge of a bond shelf to interconnect a power bus to one or more bond pads on the shelf. The conductive strip is typically formed by initially masking all surfaces of the integrated circuit package except for the edge, and then dipping the package into a plating bath of copper. The plating bath plates copper onto the edge on the bond shelf.

The conductive copper strip extends continuously along the entire edge of the bond shelf. Because of this only one voltage level can be supplied to the contact pads located on the bond shelf with the plated edge. To provide more design flexibility it would be desirable to connect multiple power/ground planes to the bond pads on the bond shelf with the conductive strip.

SUMMARY OF THE INVENTION

The present invention is an electronic package that may include a first bond pad and a second bond pad located on a bond shelf. The bond shelf may have an edge. The package may have a first conductive bus that may be connected to the first bond pad by a first conductive strip that extends along the edge of the bond shelf. The package may also have a second conductive bus that may be connected to the second bond pad by a second conductive strip that extends along the edge of the bond shelf.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of an integrated circuit package of the present invention;

Figure 2 is a top sectional view of the package;

Figure 3 is a top cross-sectional view of the integrated circuit package showing a pair of power busses within the same plane of the package;

Figure 4 is an enlarged perspective view of a bond shelf of the package showing a pair of conductive strips that wrap around the edge of a bond shelf to connect a pair of conductive busses to bond pads located on the shelf;

Figure 5 is a perspective view showing the package masked by a plating resist material;

Figure 6 is a side view showing the package within a plating bath;

Figure 7 is an enlarged view of a conductive strip that extends along an edge of a bond shelf.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings more particularly by reference numbers, Figures 1-3 show an integrated circuit package 10 of the present invention. Mounted to the package 10 is an integrated circuit 12. Although an integrated circuit 12 is shown and described, it is to be understood that the package 10 may house any passive or active electrical device. The integrated circuit 12 has a plurality of bond pads 14 that are connected to corresponding bond pads 16 of a package housing 11. The bond pads 14 and 16 may be connected by bond wires 17 or a tape automated bonding (TAB) tape (not shown). The bond pads 16 may be located on a first bond shelf 18, a second bond shelf 20 and a third bond shelf 22. Although three bond shelves are shown and described, it is to be understood that the package 10 may have any number of bond shelves.

The bond pads 16 of the first bond shelf 20 are connected to a pair of power busses 24 and 26 within the package. The busses 24 and 26 are separated and located within the same horizontal plane of the package. By locating both power busses 24 and 26 within the same plane the present invention provides a package that may require less layers than a package that has two power busses located within different layers of the package.

The package 10 may also have one or more layers of routing traces 28 and a ground bus 30 dedicated to the

digital signal lines and ground of the integrated circuit 12, respectively. The busses 24, 26 and 30, and traces 28 are connected to a plurality of contacts 32 that are attached to surface pads 33 located on a bottom surface of the package 10. The contacts 32 may be solder balls that are reflowed onto a printed circuit board 34. By way of example, the printed circuit board 34 may be a motherboard of a computer that contains a power supply(ies) 36 that provides two different voltage levels of power.

In one embodiment, the power bus 24 is connected to one voltage level, such as 3.3 V, and the other power bus 26 can be connected to a second voltage level, such as 2.0 V. In this manner the package provides two different voltage levels to the integrated circuit 12. Although the busses 24 and 26 are described as being both dedicated to power, it is to be understood that one bus may be connected to power and the other bus may be connected to ground. Such a configuration may reduce the capacitance of the package 10. Additionally, although solder balls 32 are shown and described, it is to be understood that the package 10 may have other types of contacts such as pins (not shown) that are soldered to the printed circuit board 34.

The bond pads 16, contacts 32 and layers 24, 26, 28, 30 and 32 may all be interconnected by vias 38. The busses 24 and 26 may include clearance spaces 42 that electrically isolate the busses 24 and 26 from the vias 38. Additionally, the busses 24 and 26 are also separated by spaces 43.

Figure 4 shows a first conductive strip 44 and a second conductive strip 46 that wrap around an edge of the first bond shelf 20 to connect the bond pads 16 to the power busses 24 and 26. The conductive strips 44 and 46 can be separated by a pair of notches 48 formed in the first bond shelf 20. Some of the bond pads 16 are connected by strip 44 to bus 24 while other bond pads 16 are connected to bus 26 by strip 46. The separate strips allow the bond pads 16 on the first shelf 18 to be connected to two different voltage levels. The other bond pads 16 on the first shelf 20 are interconnected to other layers and/or contacts 34 by vias 38.

In the preferred embodiment, the package 10 is constructed with a laminated printed circuit board process. The ground layer 30 can be formed on a dielectric substrate with conventional photolithographic techniques. A second substrate may be placed on the ground layer 30. The layer may have a plurality of holes used for the formation of the vias 38. The second substrate may contain copper layers that are etched to form the routing traces 28 and bond pads 16. Additional substrates may be added to create the busses 24 and 26, and bond pads 16. The vias 38 can then be formed with a plating process. The substrates are then "auto-claved" to form the package housing 11.

The conductive strips 44 and 46 can be formed by initially masking off all surfaces of the package housing, except the edge of the third shelf 22 with a plating resist maskant 50, as shown in Figure 5. The masked housing can

then be dipped into a plating bath 52 as shown in Figure 5. The plating bath 52 plates a conductive material such as copper onto the edge of the first bond shelf 18. The maskant 50 is then removed and the notches 48 can be drilled into the edges of the first bond shelf 18 to separate the plated material into the first and second conductive strips 44 and 46. All exposed copper surfaces may then be plated with gold.

As shown in Figure 7, portions 54 of the conductive strips 44 and 46 may extend onto the first bond shelf 18. The extra portions 54 may further anchor the conductive strips 44 and 46 to the housing and reduce the likelihood of delamination during the drilling process. The additional portions 54 can be formed by not masking the end of the first bond shelf 18 so that conductive material plates onto the shelf.

Referring to Figs. 1 and 2, after the strips 44 and 46 are formed, the integrated circuit 12 may be mounted onto the package and connected to the bond pads 16. The integrated circuit 12 may then be enclosed with an encapsulant 56. The contacts 32 are attached to the surface pads 33 to complete the package 10.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and

arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

What is claimed is:

1. An electronic package, comprising:

a housing that has a first bond shelf and an edge;

a first bond pad located on said first bond shelf;

a second bond pad located on said first bond shelf

a first conductive bus located within said housing;

a first conductive strip that wraps around said edge and connects said first conductive bus to said first bond pad;

a second conductive bus located within said housing; and,

a second conductive strip that wraps around said edge and connects said second conductive bus to said second bond pad.

2. The package as recited in claim 1, wherein said first and second conductive strips extend onto said first bond shelf.

3. The package as recited in claim 1, wherein said first bond shelf edge includes a notch that separates said first conductive strip from said second conductive strip.

4. The package as recited in claim 1, further comprising a third bond pad that is located on a second bond shelf.

5. The package as recited in claim 1, wherein said first conductive bus is at a first voltage potential and said second conductive bus is at a second voltage potential.

6. The package as recited in claim 1, further comprising an integrated circuit that is mounted to said housing and connected to said first and second bond pads.

7. An electronic package, comprising:

a housing that has a first bond shelf that has an edge;

a first bond pad located on said bond pad shelf;

a first conductive strip that extends along said edge and onto said bond shelf.

8. The package as recited in claim 7, further comprising a second bond pad located on said first bond shelf, and a second conductive bus that is connected to said second bond pad by a second conductive strip that wraps around said edge and extends onto said first bond shelf.

9. The package as recited in claim 8, wherein said first bond shelf edge includes a notch that separates said first conductive strip from said second conductive strip.

10. The package as recited in claim 8, further comprising a third bond pad that is located on a second bond shelf.

11. The package as recited in claim 8, wherein said first conductive bus is at a first voltage potential and said second conductive bus is at a second voltage potential.

12. The package as recited in claim 7, further comprising an integrated circuit that is mounted to said housing and connected to said first bond pad.

13. A method for assembling an electronic package, comprising:

forming a housing which has a bond pad located on a bond shelf which has an edge;

forming a conductive strip along the edge of the bond shelf;

removing a portion of the conductive strip.

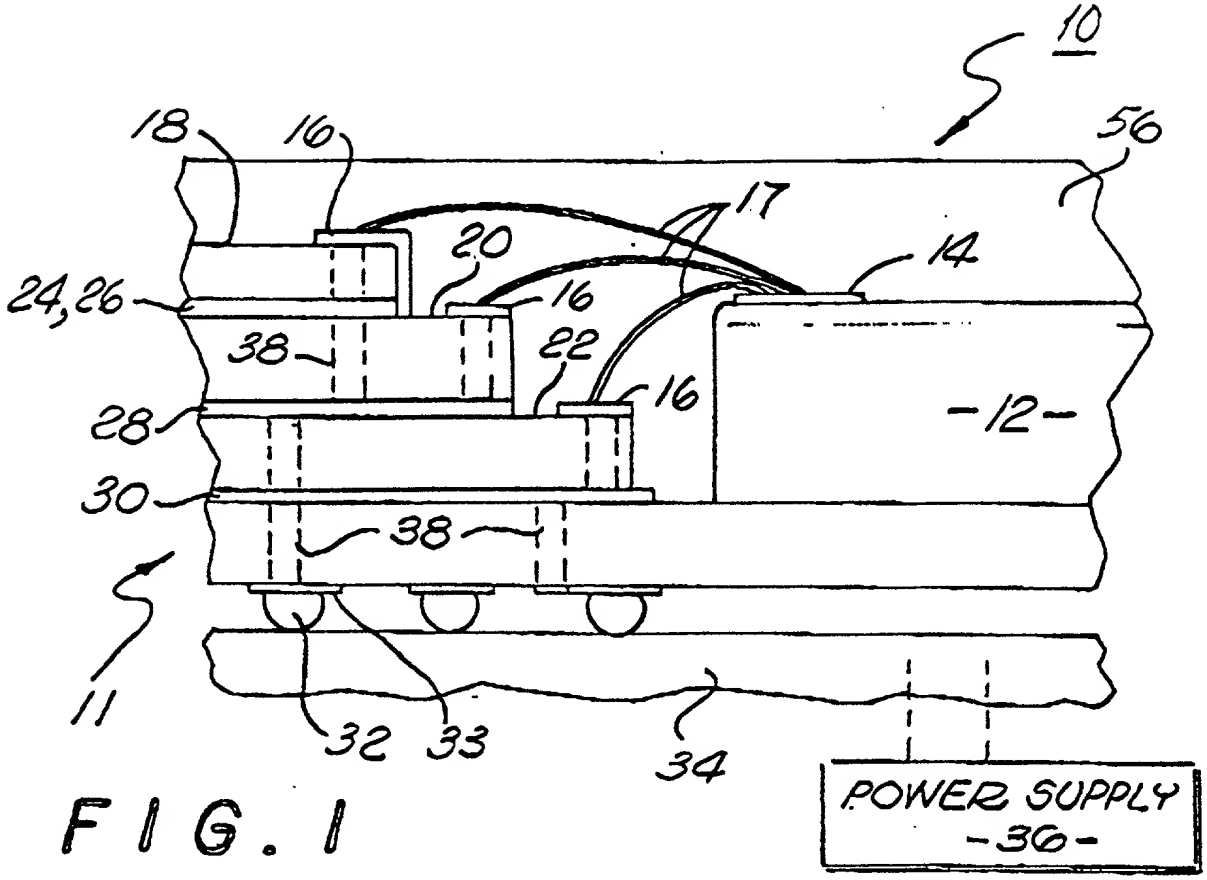
14. The method as recited in claim 13, wherein the conductive strip is formed by plating a conductive material onto the edge.

15. The method as recited in claim 13, wherein the portion of the conductive material is removed by drilling a portion of the bond shelf.

16. The package as recited in claim 13, further comprising the steps of mounting an integrated circuit to the housing and connecting the integrated circuit to the bond pad.

ABSTRACT OF THE DISCLOSURE

An electronic package that may include a first bond pad and a second bond pad located on a bond shelf. The bond shelf may have an edge. The package may have a first conductive bus that may be connected to the first bond pad by a first conductive strip that extends along the edge of the bond shelf. The package may also have a second conductive bus that may be connected to the second bond pad by a second conductive strip that extends along the edge of the bond shelf.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POWER SUPPLY
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FIG. 1

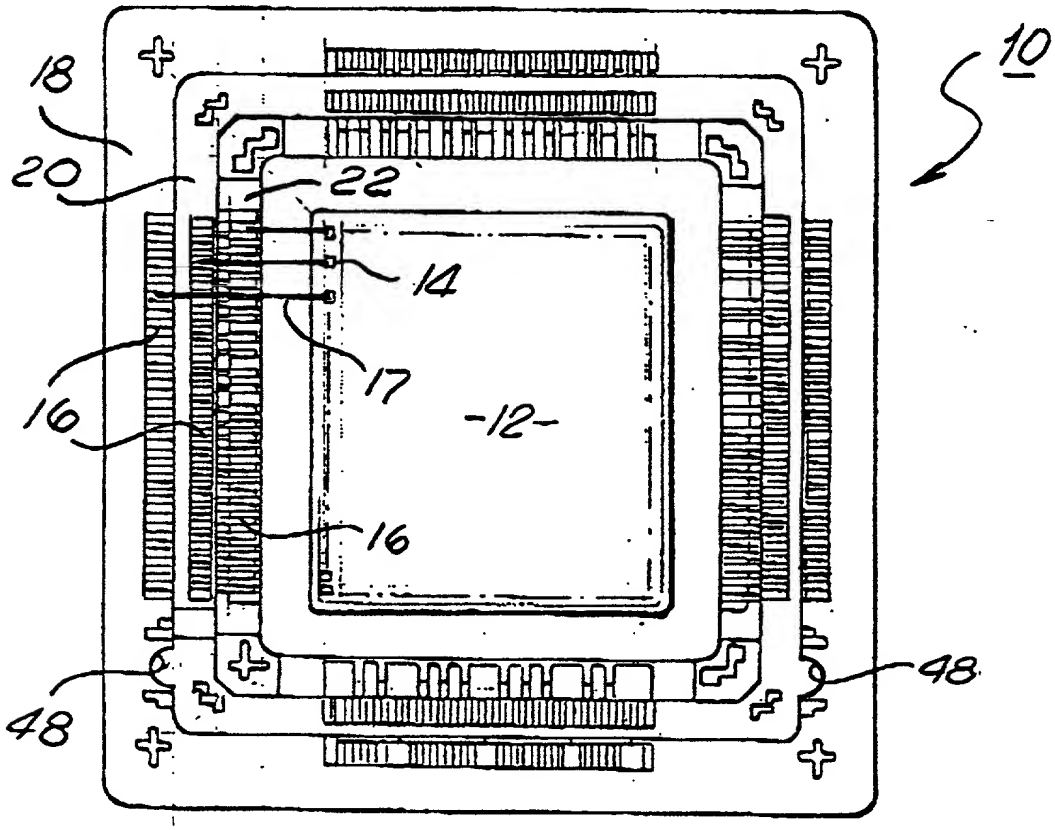
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FIG. 2

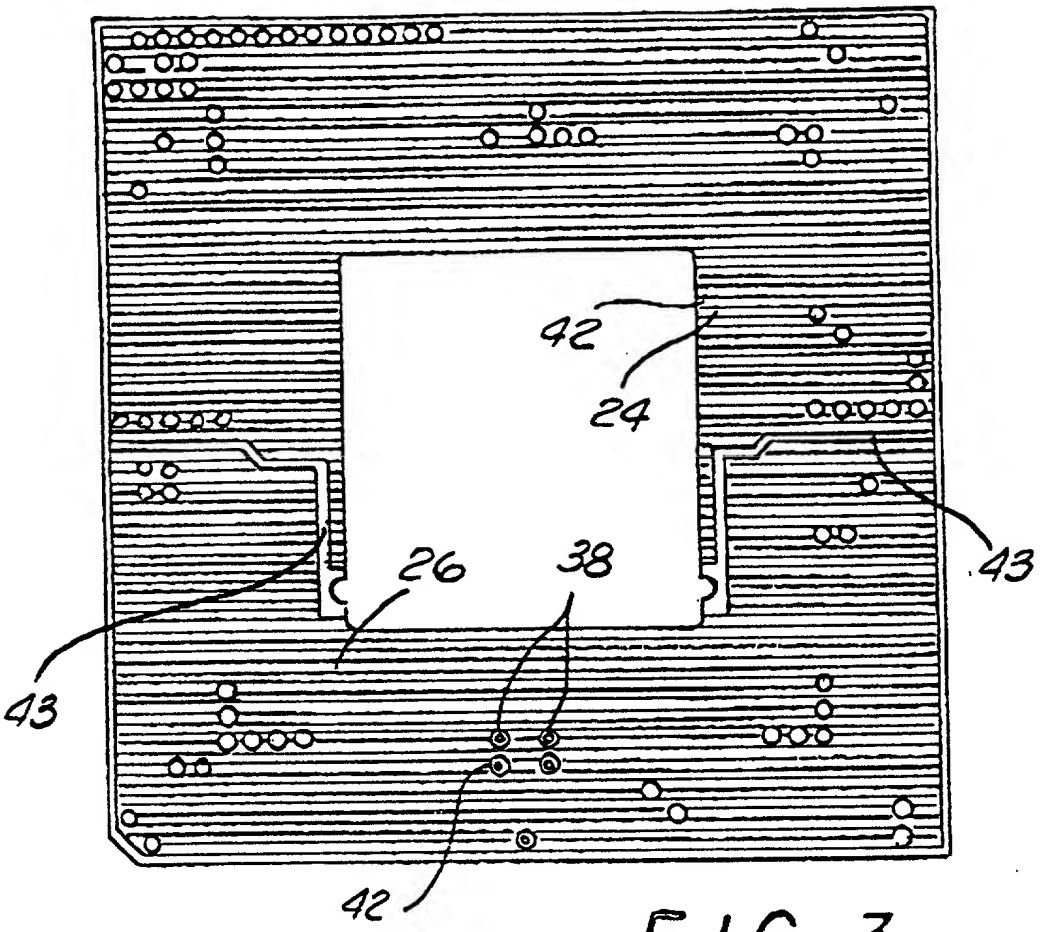

FIG. 3

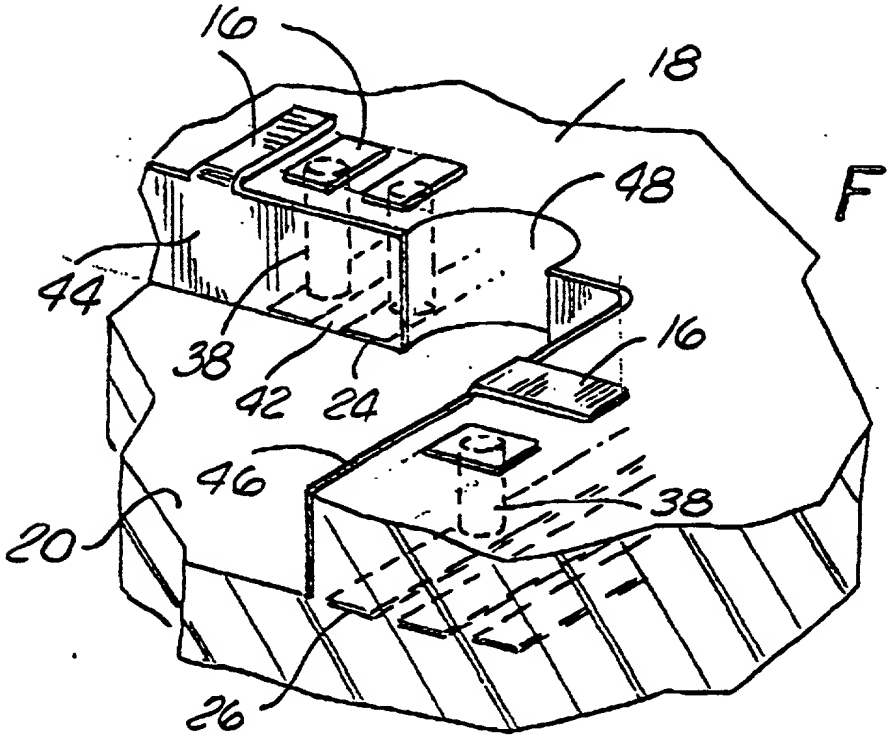

FIG. 4

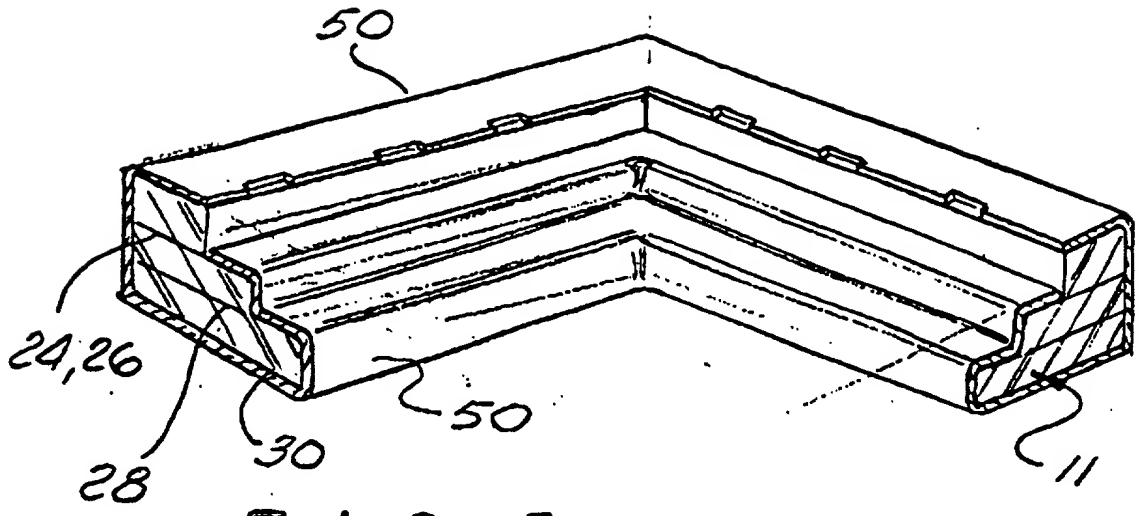

FIG. 5

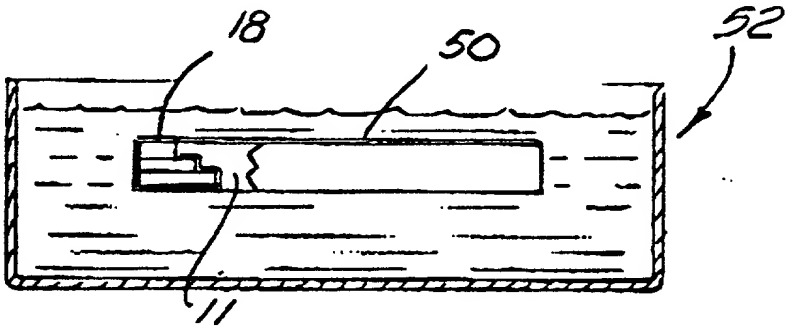

FIG. 6

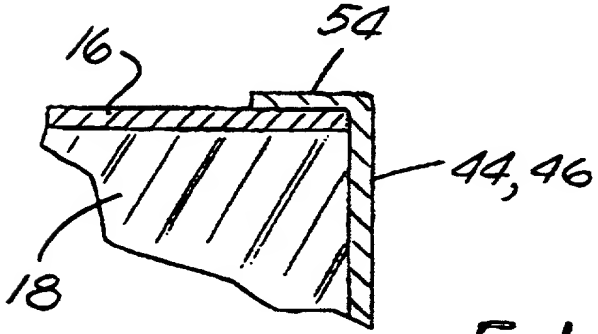

FIG. 7

Attorney's Docket No.: 042390.P6139

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint-inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SPLIT CAVITY WALL PLATING FOR AN INTEGRATED CIRCUIT PACKAGE

the specification of which

[X] is attached hereto.
[ ] was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____ .
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the

prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, a firm including: Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, P41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. P42,442; William Donald Davis, Reg. No. 38,428; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Tarek N. Fahmi, Reg. No. P41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., P42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, P41,839; Willmore F. Holbrow III, Reg No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Tim L. Kitchen, Reg. No. P41,900; Michael J. Mallie, Reg. No. 36,591; Paul A. Mendonsa P42,879; Darren J. Milliken, P42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch P43,021; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; Geoffrey T. Staniford, P43,151; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. P42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, P43,237; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Amy M. Armstrong, Reg. No. P42,265; Robert Andrew Diehl, Reg. No. P40,992; and Edwin A. Sloane, Reg. No. 34,728; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (714) 557-3800, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Sean Fitzgerald, Reg. No. 32,027; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,435; my patent attorneys, of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Ben J. Yorks, Reg. No. 33,609, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Ben J. Yorks, Reg. No. 33,609, (714) 557-3800.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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